IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 4 (Cancelled)

5. (New) A semiconductor integrated circuit device comprising:

a logic circuit including at least a first MIS transistor;

a monitoring circuit including at least a second MIS transistor to output an oscillation signal,

a substrate bias voltage generator to supply a substrate bias voltage to the first MIS transistor and the second MIS transistor; and

a comparator to compare a reference clock signal and the oscillation signal,

wherein the substrate bias voltage generator changes the substrate bias voltage on a predetermined voltage unit basis in accordance with a result of a comparison operation of the comparator.

6. (New) The semiconductor integrated circuit device according to claim 5,

wherein the comparator outputs a first control signal when a delay difference of the oscillation signal from the reference clock signal is faster than a predetermined value and the comparator outputs a second control signal when the delay difference is slower than the predetermined value.

7. (New) The semiconductor integrated circuit device according to claim 6,

wherein the substrate bias voltage generator controls the substrate bias voltage so as to increase absolute threshold values of the first and second MIS transistors, when the substrate bias voltage receives the first control signal, and

wherein the substrate bias voltage generator controls the substrate bias voltage so as to decrease the absolute threshold values of the first and second MIS transistors, when the substrate bias voltage generator receives the second control signal.

8. (New) The semiconductor integrated circuit device according to claim 7,

wherein the substrate bias generator includes a digital-to-analog converter and a plural stages of registers having plural register positions to the digital-to-analog converter,

wherein the digital-to-analog converter outputs the substrate bias voltage according to the register position, and

wherein the register position is changed according to whether the substrate bias generator receives the first control signal or the second control signal.

9. (New) The semiconductor integrated circuit device according to claim 7,

wherein the substrate bias generator includes a first digital-to-analog converter to supply the substrate bias voltage to the second MIS transistor, a second

digital-to-analog converter to supply the substrate bias voltage to the first MIS transistor and first plural stages of registers having plural first register positions to the first digital-to-analog converter,

wherein the first digital-to-analog converter outputs the substrate bias voltage to the second MIS transistor according to the first register position, and,

wherein the first register position is changed according to whether the substrate bias generator receives the first control signal or the second control signal.

10. (New) The semiconductor integrated circuit device according to claim 9,

wherein the second digital-to-analog converter supplies the substrate bias voltage that has the same value as the first digital-to-analog converter.

11. (New) The semiconductor integrated circuit device according to claim 5,

wherein the monitoring circuit includes a plurality of inverters connected in series, and

wherein each of the plurality of inverters includes the second MIS transistor.

12. (New) A semiconductor integrated circuit device, comprising:

a logic circuit including at least a first MIS transistor, wherein subthreshold leakage current flows through the first MIS transistor; and

a control circuit to control an operating speed of the logic circuit,

wherein the control circuit changes a voltage to supply to the first MIS transistor on a predetermined voltage unit basis,

wherein the subthreshold leakage current of the first MIS transistor increases when the control circuit increases the operating speed of the logic circuit, and

wherein the subthreshold leakage current of the first MIS transistor decreases when the control circuit decreases the operating speed of the logic circuit.

13. (New) The semiconductor integrated circuit device according to claim 12,

wherein the control circuit includes a monitoring circuit including at least a second MIS transistor to output an oscillation signal and a comparator to compare a reference clock signal and the oscillation signal, and

wherein the control circuit supplies the voltage to the first MIS transistor and the MIS second transistor, and wherein the control circuit changes the voltage on A predetermined voltage unit basis in accordance with a result of A comparison operation of the comparator.

14. (New) The semiconductor integrated circuit device according to claim 13,

wherein the voltage is a substrate bias voltage, and

wherein the control circuit includes a substrate bias voltage generator to supply the substrate bias voltage to the first MIS transistor and the second MIS transistor.

15. (New) The semiconductor integrated circuit device according to claim 14,

wherein the comparator outputs a first control signal when a delay difference of oscillation signal from the reference clock signal is faster than a predetermined value and the comparator outputs a second control signal when the delay difference is slower than the predetermined value.

16. (New) The semiconductor integrated circuit device according to claim 15,

wherein the substrate bias voltage generator controls the substrate bias voltage so as to increase absolute threshold values of the first and second MIS transistors, when the substrate bias voltage generator receives the first control signal, and

wherein the substrate bias voltage generator controls the substrate bias voltage so as to decrease the absolute threshold values of the first and second MIS transistors, when the substrate bias voltage receives the second control signal.

17. (New) The semiconductor integrated circuit device according to claim 16,

wherein the substrate bias generator includes a digital-to-analog converter and plural stages of registers having plural register positions to the digital-to-analog converter,

wherein the digital-to-analog converter outputs the substrate bias voltage according to the register position, and

wherein the register position is changed according to whether the substrate bias voltage generator receives the first control signal or the second control signal.

18. (New) The semiconductor integrated circuit device according to claim 13,

wherein the monitoring circuit includes a plurality of inverters connected in series, and

wherein each of the plurality of inverters includes the second MIS transistor.

19. (New) A method of controlling an operating speed of a logic circuit, comprising the steps of:

providing a semiconductor integrated circuit including the logic circuit including at least a first MIS transistor, wherein subthreshold leakage current flows through the first MIS transistor; and

controlling a voltage to supply to the first MIS transistor on a predetermined voltage unit basis to change the operating speed,

wherein the subthreshold leakage current of the first MIS transistor increases when the operating speed is controlled to increase, and

wherein the subthreshold leakage current of the first MIS transistor decreases when the operating speed Is controlled to decrease.

20. (New) The method of controlling the operating speed of the logic circuit according to claim 18,

wherein the voltage is a substrate bias voltage.